issue a decryption command to a controller; and

determine a time for said assertion of said interrupt in response to said decryption command.

24. (Amended) The device of claim 22, wherein said instructions to convert said encrypted packet to said decrypted packet further includes instructions to:

parse said encrypted packet;

match said encrypted packet with a corresponding security association (SA) stored in said host memory; and

A4 cont.

transfer said encrypted packet and said corresponding SA to a controller.

25. (Amended) The device of claim 22, wherein said instructions to convert said encrypted packet to said decrypted packet further includes instructions to authenticate said decrypted packet.

26. (Amended) The device of claim 22, further including instructions to assert an additional interrupt upon completion of said transfer of said decrypted packet to said host memory.

27. (Amended) The device of claim 22, further including instructions to indicate said decrypted packet to a protocol stack after the instruction to assert said interrupt.

28. (New) A system, comprising:

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a computer to receive an encrypted packet and to perform a decryption operation that converts said encrypted packet into a decrypted packet; and

a memory included in said computer, said computer asserting an interrupt prior to a complete transfer of said decrypted packet to said memory.